

REMARKS/ARGUMENTS

Claims 1-4 are pending. No new matter has been added.

Claims 1-4 are rejected under 35 U.S.C. § 102(b) as being anticipated by (JP-2004-228553) by Torii et al.

The claims have been amended to further distinguish over the prior art. In particular, claim 1 has been amended to more clearly set forth that a first region of third semiconductor regions have a first area and are formed in a center of the semiconductor base and a second region of third semiconductor regions have a second area greater than the first area and are formed completely around the first region, as illustrated by example in Fig. 1. Furthermore, the third semiconductor regions comprise a dual stacked structure of a first device stacked atop a second device, as illustrated by example in Fig. 5. Claim 1 as amended recites in part:

A semiconductor device, comprising:
a semiconductor base comprising a plurality of first semiconductor regions having a first conductivity type, a plurality of second semiconductor regions having a second conductivity type formed in a specific surface portion of said first semiconductor regions, and a plurality of third semiconductor regions having the first conductivity type formed in a specific surface portion of said second semiconductor regions; and
a first electrode formed directly above said second semiconductor region that is between said first semiconductor region and said third semiconductor regions,
wherein a first region comprising a first plurality of third semiconductor regions exhibiting a first surface area is formed at a center of said semiconductor base,
wherein a second region comprising a second plurality of third semiconductor regions exhibits a second surface area larger than said first surface area completely surrounds said first region.
wherein said first plurality of third semiconductor regions and said second plurality of third semiconductor regions, each comprise a first device stacked on top of a second device.

(emphasis added). No new matter has been added.

JP-2004-228553 does not disclose “a second region [of 3rd semiconductor regions]... completely surrounds said first region[of 3rd semiconductor regions].” The JP reference further does not disclose “wherein said first plurality of third semiconductor regions and said second plurality of third semiconductor regions, each comprise a first device stacked on top of a second device.”

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance and an action to that end is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 650-326-2400.

Respectfully submitted,

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